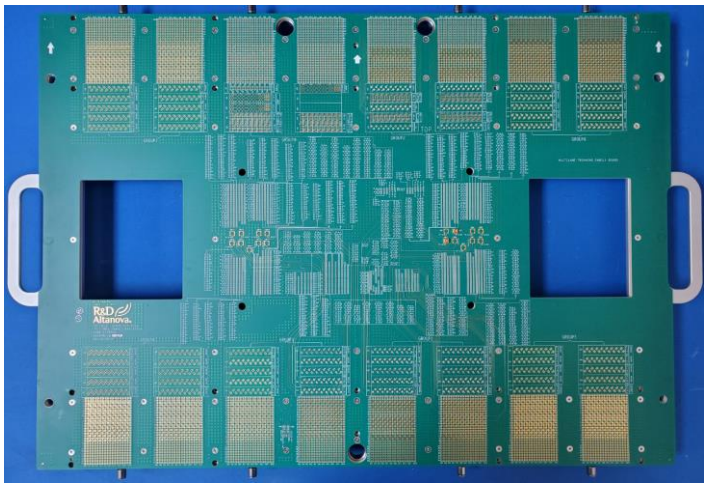
USER MANUAL

multiLane

AT93000-1900002 User Manual

Family Board Overview to help with DUT Loadboard Development

User Manual Revision 0.4, April 2022



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Notices

General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the General Safety Summary in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Only use the power cord specified for this product and certified for the country of use.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal that exceeds the maximum rating of that terminal.

Do Not Operate Without Covers.

Do not operate this product with covers or panels removed.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate with Suspected Failures.

If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions. Do Not Operate in an Explosive Atmosphere. Keep Product Surfaces Clean and Dry

⚠ *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Contents

Table of Figures

Purpose of this User Manual

A “device under test” (DUT) loadboard will be designed by the test engineer – either a package test loadboard or a wafer test loadboard. Since the tester resources come up through the twinning frame via the Family Board, this AT93000-1900002 Family Board User Manual can be used to determine the pin assignments for the DUT PCB Loadboard.

The following is provided to help design a DUT PCB loadboard for the AT93000 twinning frame:

1) A mechanical outline and DXF files with V93K resource landing pad coordinate locations on the PCB: Visit the Advantest TDC at AT93000 Package and Probe PCB information
2) A detailed pin list Excel file for the AT93000-1900002 family board is located on the MultiLane public website at AT93000-1900002
3) This AT93000-1900002 Family Board User Guide: An overview of pin mapping from V93K tester resources, through the Family Board, through the Advantest Pogo Blocks, and ultimately to the DUT PCB loadboard landing pads.

Overview of the Advantest V93000 High Speed I/O (HSIO) Test System

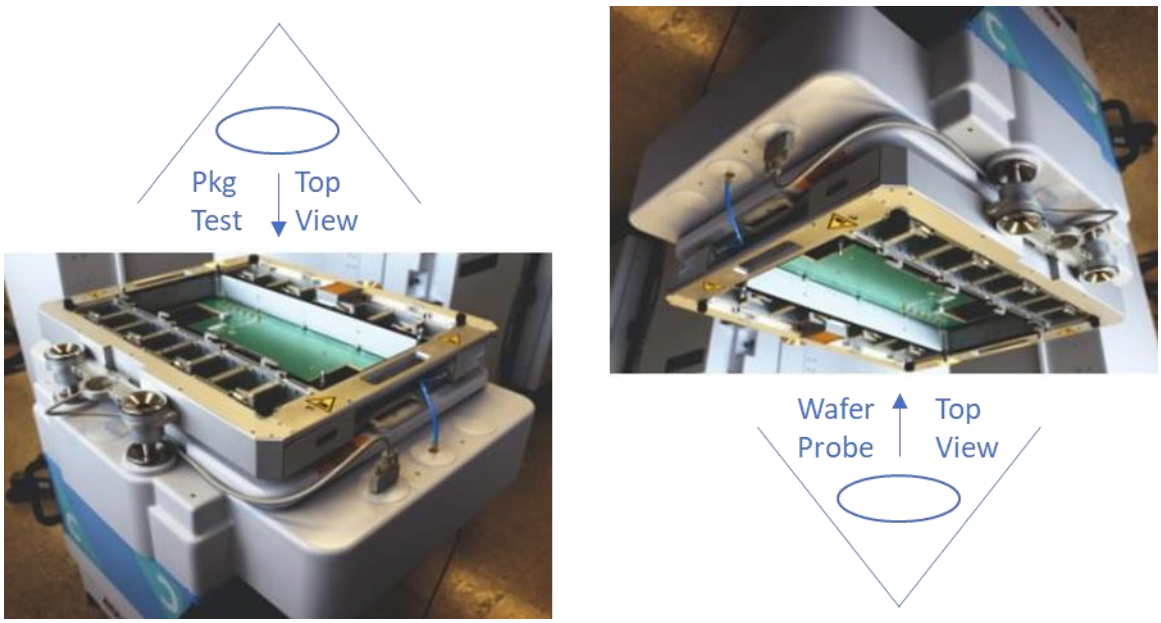


Figure 1: V93k CTH testhead with MultiLane AT93000 system attached on top

In Figure 1, the AT93000 twinning system is hard docked on top of a V93000 (V93K) test head. The AT93000 is compatible with CTH and STH Advantest V93K testheads. In the case of package test, the user’s DUT loadboard is hard docked on top of the AT93000 system and the device handler is hard docked on top of the DUT loadboard. For wafer probe, the AT93000 system would be upside down from this picture and would be hard docked to the wafer prober at the bottom of this picture. Figure 1 shows the AT93000 twinning frame with the green-colored Family Board and one Pogo Segment. The DUT loadboard is not shown in this picture.

Note: “Top View” references in this manual are defined by Figure 1.

Overview of the Family Board

An exploded view of the AT93000 twinning frame assembly is shown in Figure 2. The family board is the bottom green PCB of Figure 2.

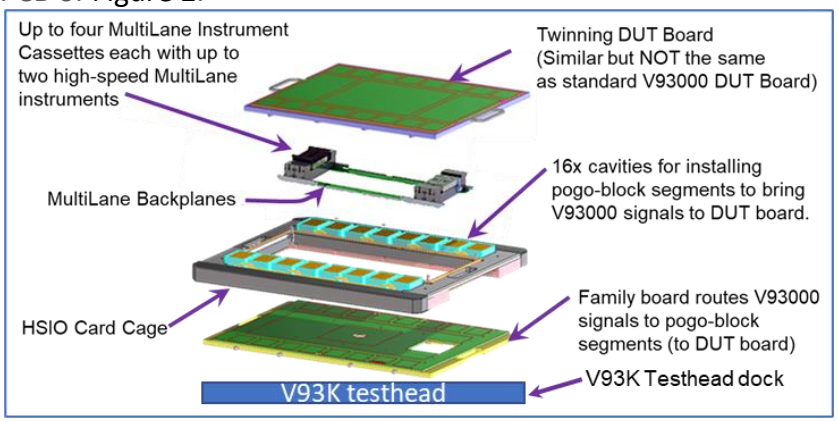


Figure 2: Building blocks of the MultiLane AT93000 system

The Family board's function is to deliver the Advantest V93K testhead resources through the HSIO Card Cage, via the pogo block groups 1A through 8B, up to the DUT loadboard. The 16 HSIO card cage cavities around the perimeter of the AT93000 system are labeled in Figure 3. Any number of these 16 cavities will be populated with a Pogo Block.

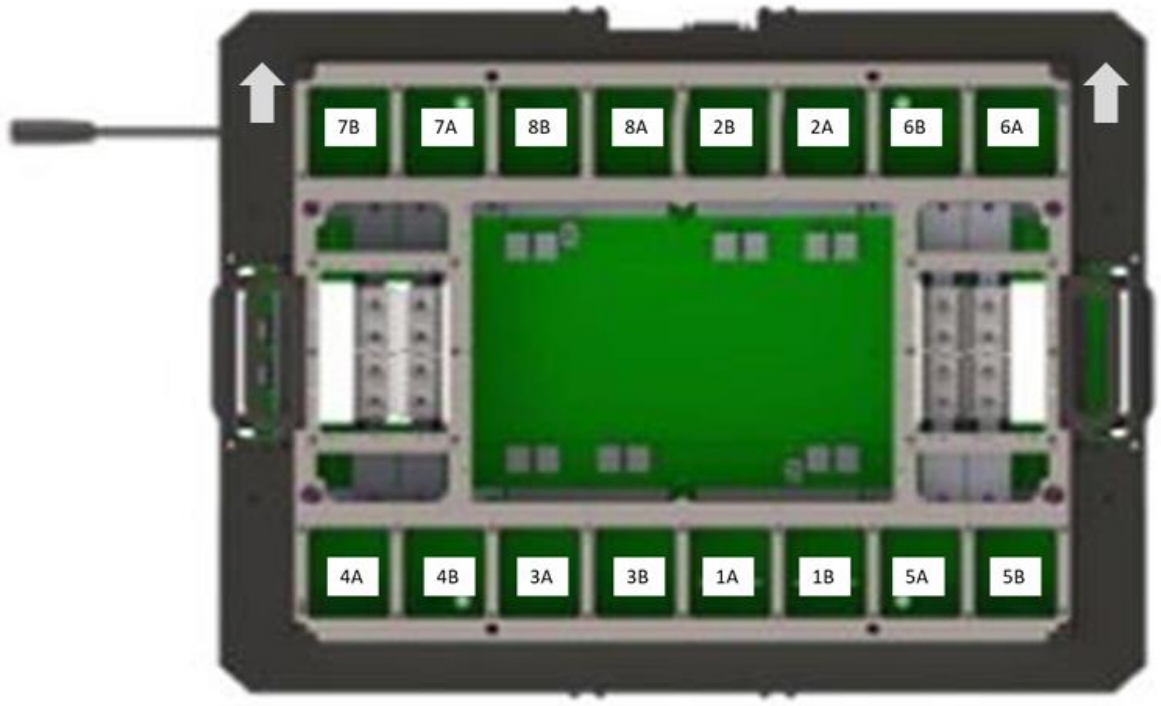


Figure 3: (Top View) AT93000 system

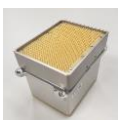


Figure 4: Pogo Block loads into 1 of 16 groups. Ordered through Advantest. P/N E8028PSD

V93K mapped resources delivered through the AT93000-1900002 are as follows[1]:

- 11x PS1600 (1408 pins)
- 3x PS9G (192 pins)
- 4x DPS64 (256 supplies)
- 2x DPS128 (256 supplies)
- 2x UHC4 (8 supplies @ 40A)
- 1x MBAV8

Find additional tester resource information on page 8.

Referring to Figure 3, Groups 7B,7A,8B,8A,2B,2A,6B,6A are referred to here as the "top-row" (top view). Groups 4A,4B,3A,3B,1A,1B,5A,5B are referred to here as the "bottom-row" (top view).

Referring to Figure 3, the [top view] pin coordinates for bottom-row and top-row pogo blocks are shown in Figure 5.

Note: Top-Row and Bottom-Row signal pin coordinates are rotated 180 degrees with respect to each other.

Note: The extra detail shown in Figure 6 and Figure 7 shows how some letters are skipped in this coordinate system: skipped letters are I, O, Q, S, X, and Z.

[1] AT93000-1900002 is a general-purpose custom family board. Customers may also choose to design their own custom family board to map a different configuration of V93K tester resources to their loadboard. In the case of their own custom family board, this manual's resource mapping descriptions may not apply.

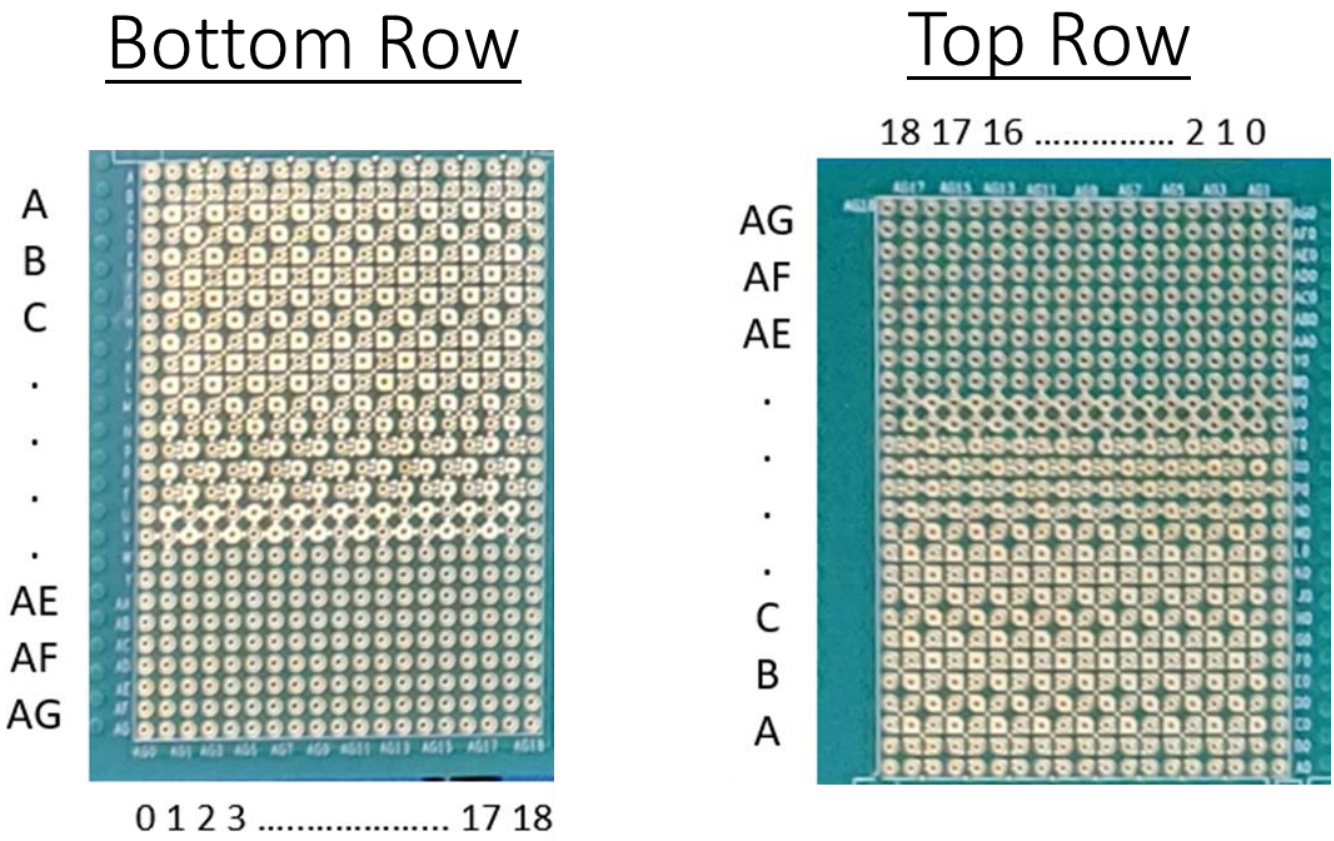


Figure 5: Signal pin coordinates for bottom and top rows (top view)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18
B	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B16	B17	B18
C	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15	C16	C17	C18
D	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18
E	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13	E14	E15	E16	E17	E18
F	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16	F17	F18
G	G0	G1	G2	G3	G4	G5	G6	G7	G8	G9	G10	G11	G12	G13	G14	G15	G16	G17	G18
H	H0	H1	H2	H3	H4	H5	H6	H7	H8	H9	H10	H11	H12	H13	H14	H15	H16	H17	H18
J	J0	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16	J17	J18
K	K0	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16	K17	K18
L	L0	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12	L13	L14	L15	L16	L17	L18
M	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12	M13	M14	M15	M16	M17	M18
N	N0	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16	N17	N18
P	P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	P16	P17	P18
R	R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	R17	R18
T	T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	T17	T18
U	U0	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	U14	U15	U16	U17	U18
V	V0	V1	V2	V3	V4	V5	V6	V7	V8	V9	V10	V11	V12	V13	V14	V15	V16	V17	V18
W	W0	W1	W2	W3	W4	W5	W6	W7	W8	W9	W10	W11	W12	W13	W14	W15	W16	W17	W18
Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	Y10	Y11	Y12	Y13	Y14	Y15	Y16	Y17	Y18
AA	AA0	AA1	AA2	AA3	AA4	AA5	AA6	AA7	AA8	AA9	AA10	AA11	AA12	AA13	AA14	AA15	AA16	AA17	AA18
AB	AB0	AB1	AB2	AB3	AB4	AB5	AB6	AB7	AB8	AB9	AB10	AB11	AB12	AB13	AB14	AB15	AB16	AB17	AB18
AC	AC0	AC1	AC2	AC3	AC4	AC5	AC6	AC7	AC8	AC9	AC10	AC11	AC12	AC13	AC14	AC15	AC16	AC17	AC18
AD	AD0	AD1	AD2	AD3	AD4	AD5	AD6	AD7	AD8	AD9	AD10	AD11	AD12	AD13	AD14	AD15	AD16	AD17	AD18
AE	AE0	AE1	AE2	AE3	AE4	AE5	AE6	AE7	AE8	AE9	AE10	AE11	AE12	AE13	AE14	AE15	AE16	AE17	AE18
AF	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15	AF16	AF17	AF18
AG	AG0	AG1	AG2	AG3	AG4	AG5	AG6	AG7	AG8	AG9	AG10	AG11	AG12	AG13	AG14	AG15	AG16	AG17	AG18

Figure 6: Complete signal pin coordinates, bottom row (top view) Groups 4,3,1,5

	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AG	AG18	AG17	AG16	AG15	AG14	AG13	AG12	AG11	AG10	AG9	AG8	AG7	AG6	AG5	AG4	AG3	AG2	AG1	AG0
AF	AF18	AF17	AF16	AF15	AF14	AF13	AF12	AF11	AF10	AF9	AF8	AF7	AF6	AF5	AF4	AF3	AF2	AF1	AF0
AE	AE18	AE17	AE16	AE15	AE14	AE13	AE12	AE11	AE10	AE9	AE8	AE7	AE6	AE5	AE4	AE3	AE2	AE1	AE0
AD	AD18	AD17	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
AC	AC18	AC17	AC16	AC15	AC14	AC13	AC12	AC11	AC10	AC9	AC8	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
AB	AB18	AB17	AB16	AB15	AB14	AB13	AB12	AB11	AB10	AB9	AB8	AB7	AB6	AB5	AB4	AB3	AB2	AB1	AB0
AA	AA18	AA17	AA16	AA15	AA14	AA13	AA12	AA11	AA10	AA9	AA8	AA7	AA6	AA5	AA4	AA3	AA2	AA1	AA0
Y	Y18	Y17	Y16	Y15	Y14	Y13	Y12	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
W	W18	W17	W16	W15	W14	W13	W12	W11	W10	W9	W8	W7	W6	W5	W4	W3	W2	W1	W0
V	V18	V17	V16	V15	V14	V13	V12	V11	V10	V9	V8	V7	V6	V5	V4	V3	V2	V1	V0
U	U18	U17	U16	U15	U14	U13	U12	U11	U10	U9	U8	U7	U6	U5	U4	U3	U2	U1	U0
T	T18	T17	T16	T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0
R	R18	R17	R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
P	P18	P17	P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
N	N18	N17	N16	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0
M	M18	M17	M16	M15	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0
L	L18	L17	L16	L15	L14	L13	L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	L0
K	K18	K17	K16	K15	K14	K13	K12	K11	K10	K9	K8	K7	K6	K5	K4	K3	K2	K1	K0
J	J18	J17	J16	J15	J14	J13	J12	J11	J10	J9	J8	J7	J6	J5	J4	J3	J2	J1	J0
H	H18	H17	H16	H15	H14	H13	H12	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0
G	G18	G17	G16	G15	G14	G13	G12	G11	G10	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0
F	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
E	E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
D	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
C	C18	C17	C16	C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0
B	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
A	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Figure 7: Complete signal pin coordinates, top row (top view) Groups 7,8,2,6

Family Board SMP connections

There are SMP connectors on the Family Board. That provide a path between the customer's loadboard and the Family Board, via the Advantest Pogo Blocks. This means that the loadboard and Family board can be electrically connected when the loadboard is docked to the twinning frame without having to manually connect/disconnect any cables. The SMP connectors are labeled so that it is easy to identify which pogo block pin is connected to which Family Board SMP connector. For example, in Figure 8 on page 9, the SMP silkscreen for SMP2 also has the label "TP-1A-B3".

- TP = Test Point (used for bringing DUT loadboard signals down to family board)
- 1A = POGO BLOCK 1A (see Figure 3 on page 5)
- B3 = POGO pin coordinate B3 in the POGO BLOCK (see Figure 6 on page 7)

In addition to bring single-ended signals from the loadboard, some of the SMP traces are laid out as differential pairs on the Family Board. While this is not an ideal different pair, it is the best compromise going through the digital pogo blocks.

- Differential pair traces on DUT loadboard (customer responsibility)
- POGO block pins are run as single-ended (no ability to run as differential)
- Differential pair traces on Family Board
    - SMP1/SMP2, same trace lengths
    - SMP3/SMP4, same trace lengths
    - SMP5 (no paired trace)
    - SMP6/SMP7, same trace lengths

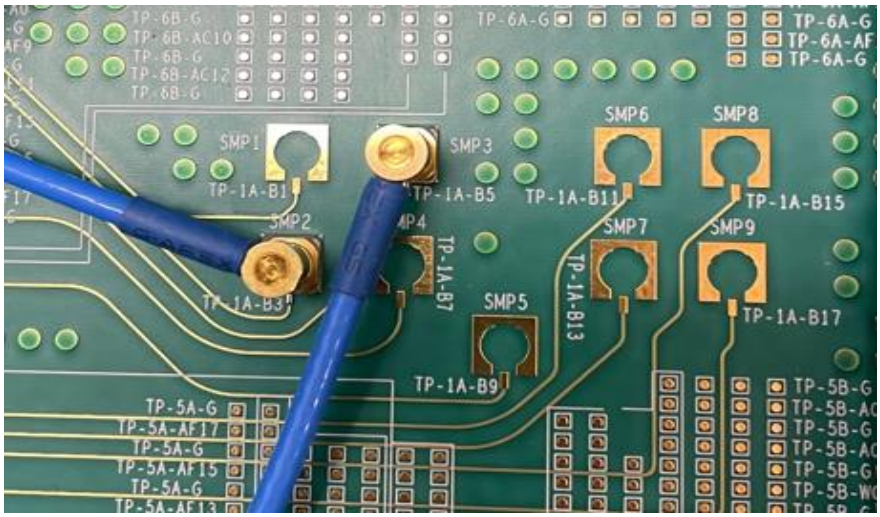


Figure 8: SMP2 and SMP3 SMP Family Board Connectors

1A		TP-1A-A14	A14		
1A		TP-1A-A16	A16		
1A		TP-1A-A18	A18		
1A		TP-1A-B1	B1	50 ohm to SMPM (Equal length traces)	
1A		TP-1A-B3	B3	50 ohm to SMPM (Equal length traces)	
1A		TP-1A-B5	B5	50 ohm to SMPM (Equal length traces)	
1A		TP-1A-B7	B7	50 ohm to SMPM (Equal length traces)	
1A		TP-1A-B9	B9	50 ohm to SMPM (Equal length traces)	
1A		TP-1A-B11	B11	50 ohm to SMPM (Equal length traces)	
1A		TP-1A-B13	B13	50 ohm to SMPM (Equal length traces)	
1A		TP-1A-B15	B15	50 ohm to SMPM (Equal length traces)	
1A		TP-1A-B17	B17	50 ohm to SMPM (Equal length traces)	
1A		TP-1A-C0	C0		
1A		TP-1A-C18	C18		
1A		TP-1A-E0	E0		

Refer to Appendix 1 on page 11 for more information about detailed pin list file.

Basically, B1 to B17 are all equal length traces, could be taken any two of them as a differential pair.

One application for this additional path is to bring a Multisite REFCLK up to the DUT loadboard or visa-versa. Figure 9 on page 9 shows how signals can be connected via the POGO BLOCK. The coax cable connection choices are arbitrary and shown for informational purposes. The populated SMP connectors on the Family Board are SMP2 and SMP3. The clock sync circuits on the MultiLane backplanes can be driven as either single-ended or differential. In this example, they are being driven as single-ended.

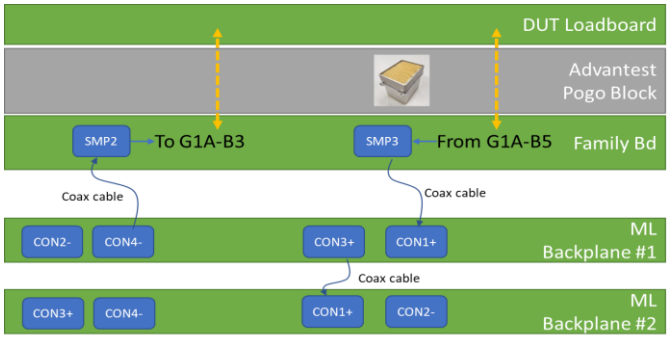


Figure 9: Example connections from DUT Loadboard to ML Backplane

The Input impedance to the CLK IN connector on the backplane AT4000 is 100 Ω.
The schematic shows a 100 Ω Single Ended to GND (R29/R30), the clock buffer requires this termination when the input is LVPECL.

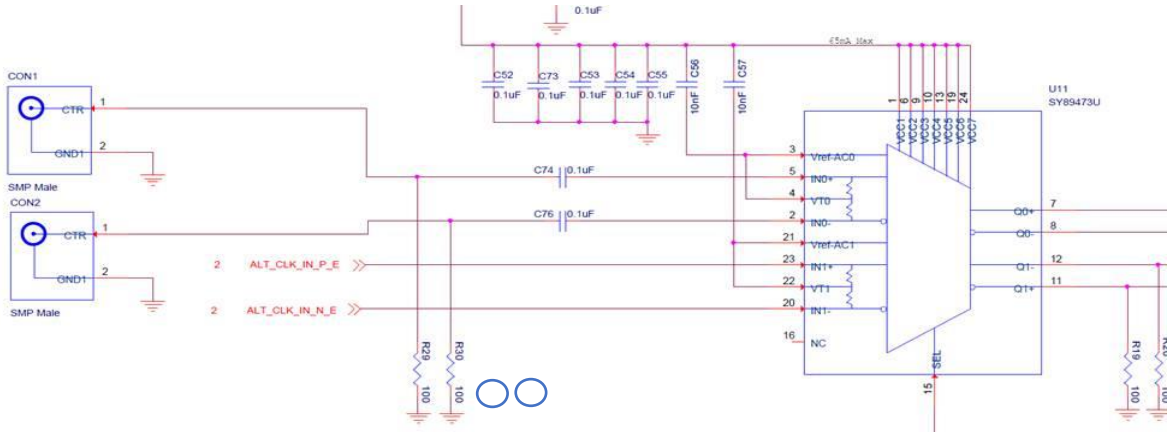


Figure 10: Clock Sync CLK IN circuit, backplanes #1 and #2

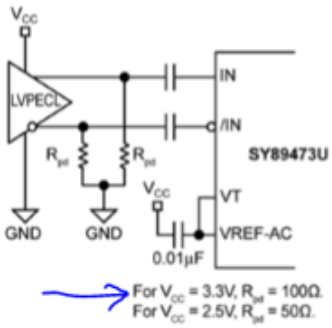


Figure 11: LVPECL Interface (AC-Coupled)

Quite often, a customer creates a clock on his loadboard using a SiLab device. The clock output from the SiLab device can travel down to the Family Board using the path just described through the POGO BLOCK.

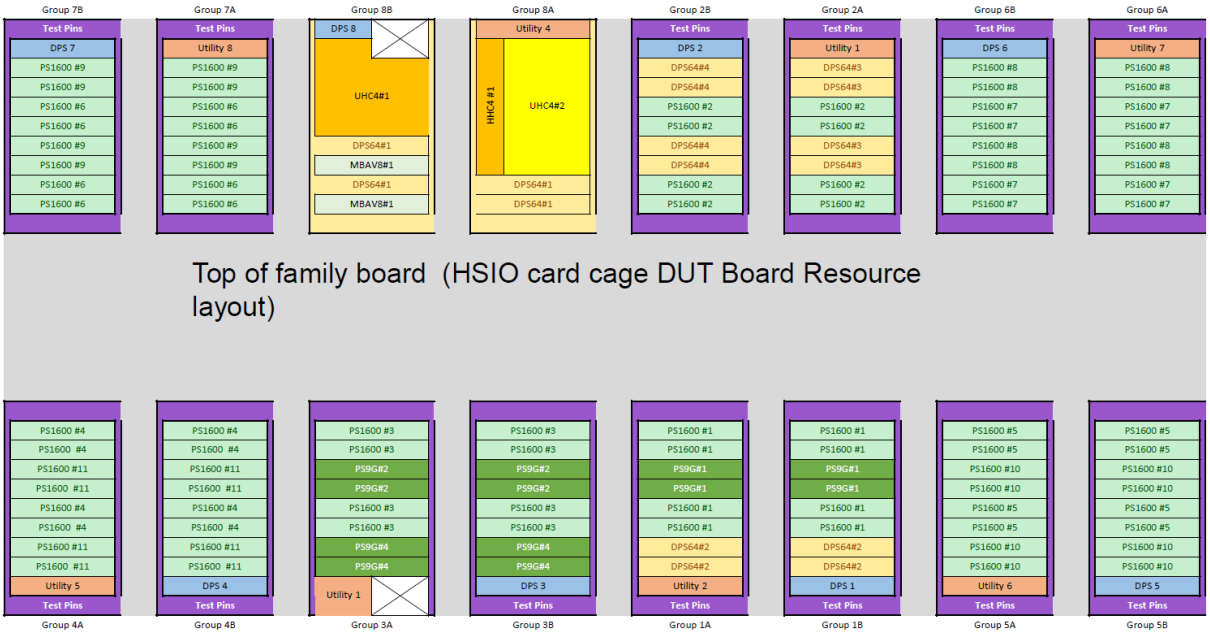
The SiLab output is usually differential LVPECL. The MultiLane clock sync will accept either a single-ended or differential input from the SiLab device.
Ideally, the SiLab output will be routed in a differential fashion to minimize the clock noise and jitter being disseminated through the backplane. However, for slower clock sync signals in the 100's of MHz, a single ended signal is often used.

Note: The impedance for the differential pair should be 100 Ω.

After the cables are connected, there are jumpers on backplane #1 and #2 that have to be configured. Instructions how to set these jumpers can be found in the AT93000 System User Manual.

Appendix 1: Additional Resource Layout Views

A detailed pin list file is on the MultiLane public website in Excel format:
AT93000-1900002 | MultiLane (MultiLaneinc.com)



Twinning Pogo Segment	PS1600		PS9G*		DPS 64/128		UHC4T		(MB)AV8+		DPS/UTIL assignment
	pin count	pogo block	pin count	pogo block	pin count	pogo block	pin count	pogo block	pin count	pogo block	
1A	64	101-104	32	301,302	32	303-304					Util 2
1B	64	105-108	32	305-306	32	307-308					DPS 1
2A	64	109-112			64	309-312					Util 3
2B	64	113-116			64	313-316					DPS 2
3A	64	117-120	64	317-320							Util 1
3B	64	121-124	64	321-324							DPS 3
4A	128	125-128 325-328									Util 5
4B	128	129-132 329-332									DPS 4
5A	128	201-204 401-404									Util 6
5B	128	205-208 405-408									DPS 5
6A	128	209-212 409-412									Util 7
6B	128	213-216 413-416									DPS 6
7A	128	217-220 417-420									Util 8
7B	128	221-224 421-424									DPS 7
8A					32	225/425	4	227/427	8	231/431	Util 4
8B					32	229/429	4	230/430			DPS 8
TOTAL	1408		192		256		8		8		

Rev. No.	Amendments		Revision date
	Section	Description	
0.1	All	Initial revision DRAFT under review	24-DEC-20
0.2	Overview of Family Board	Added link to pin list	4-JAN-21
0.3	Title Page	Updated creation date from Jan 2020 to Jan 2021	19-JAN-21
0.4	Family Board SMP Conn's	New section added	1-MAR-21